Structure

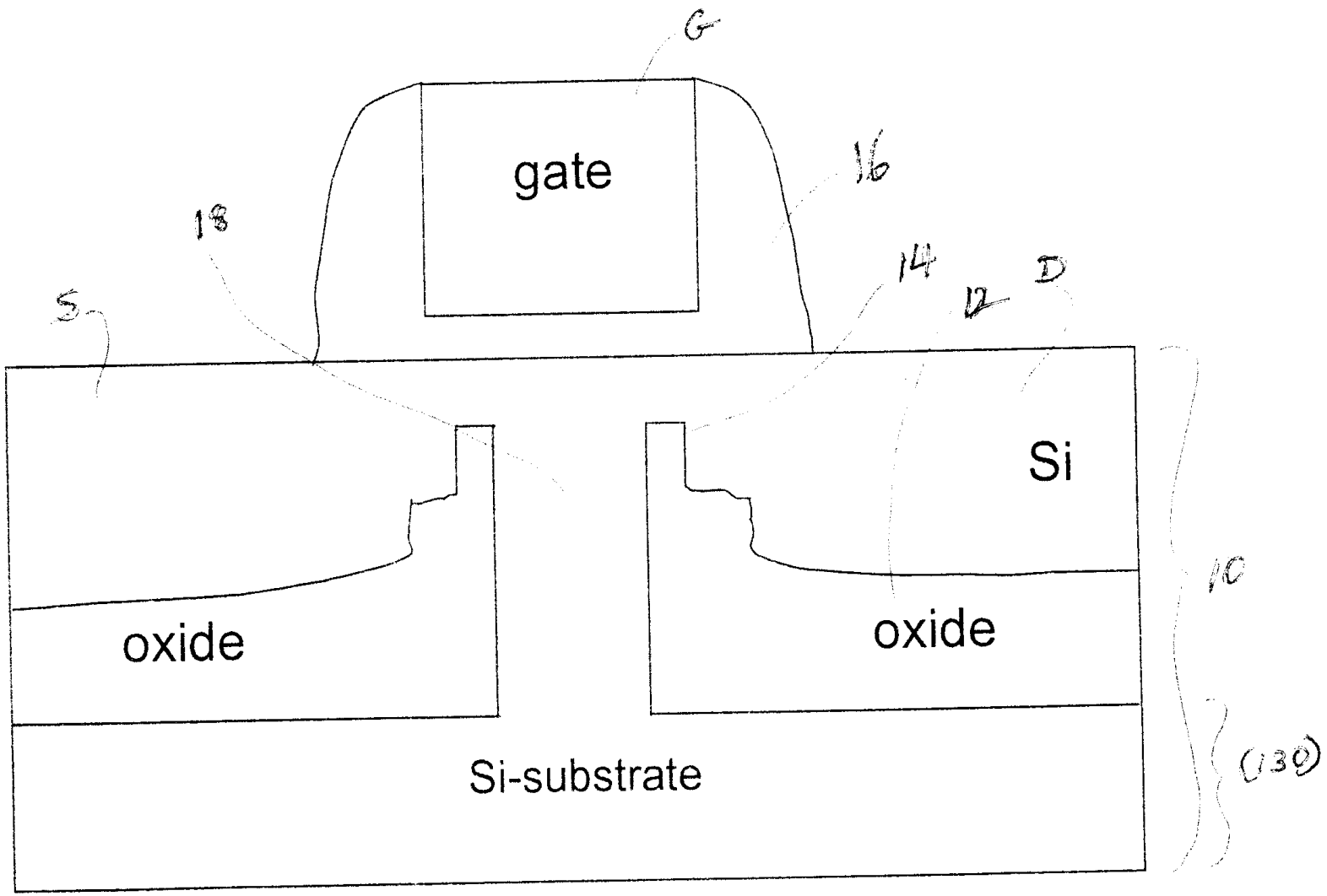


Figure 1

Step 1 Start with conventional wafer (much cheaper than SOI wafer), epi SiGe with low Ge fraction (say 10%)

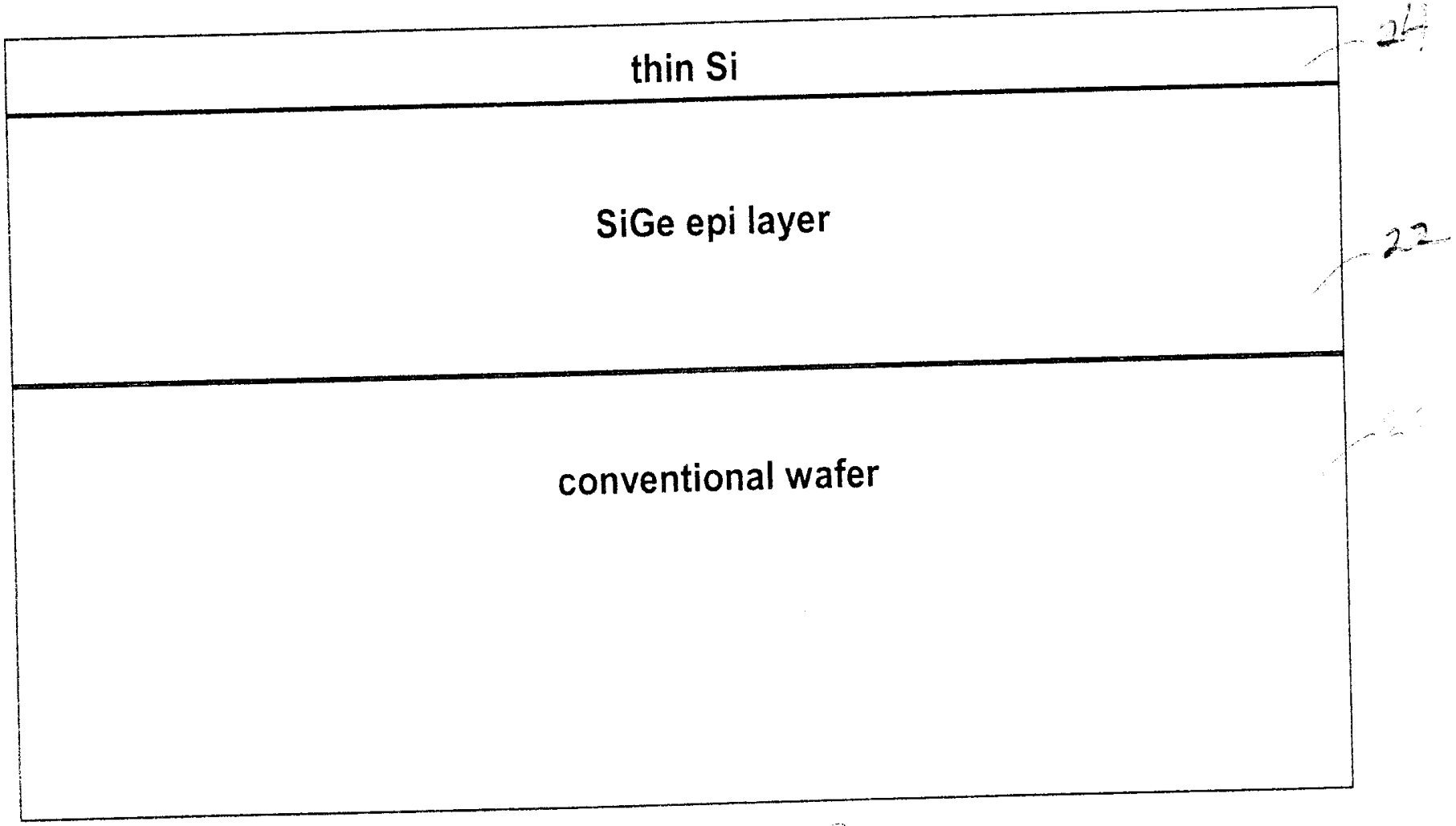


FIGURE 2

Step 2 Gate patterning followed by As ion-implantation and cover the gate and Si surface by thin nitride

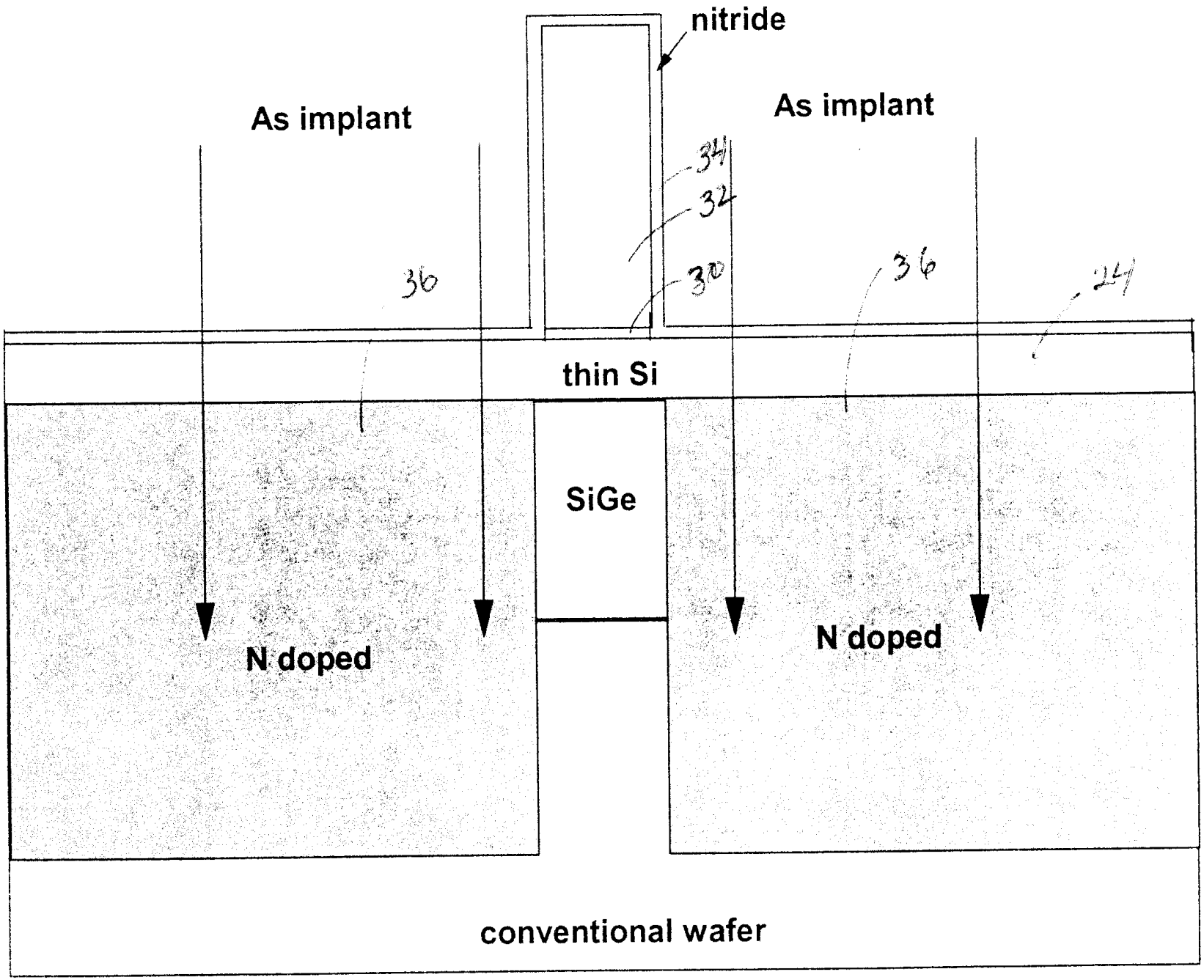


FIGURE 3

Step 3 Open trench and etch the N doped regions

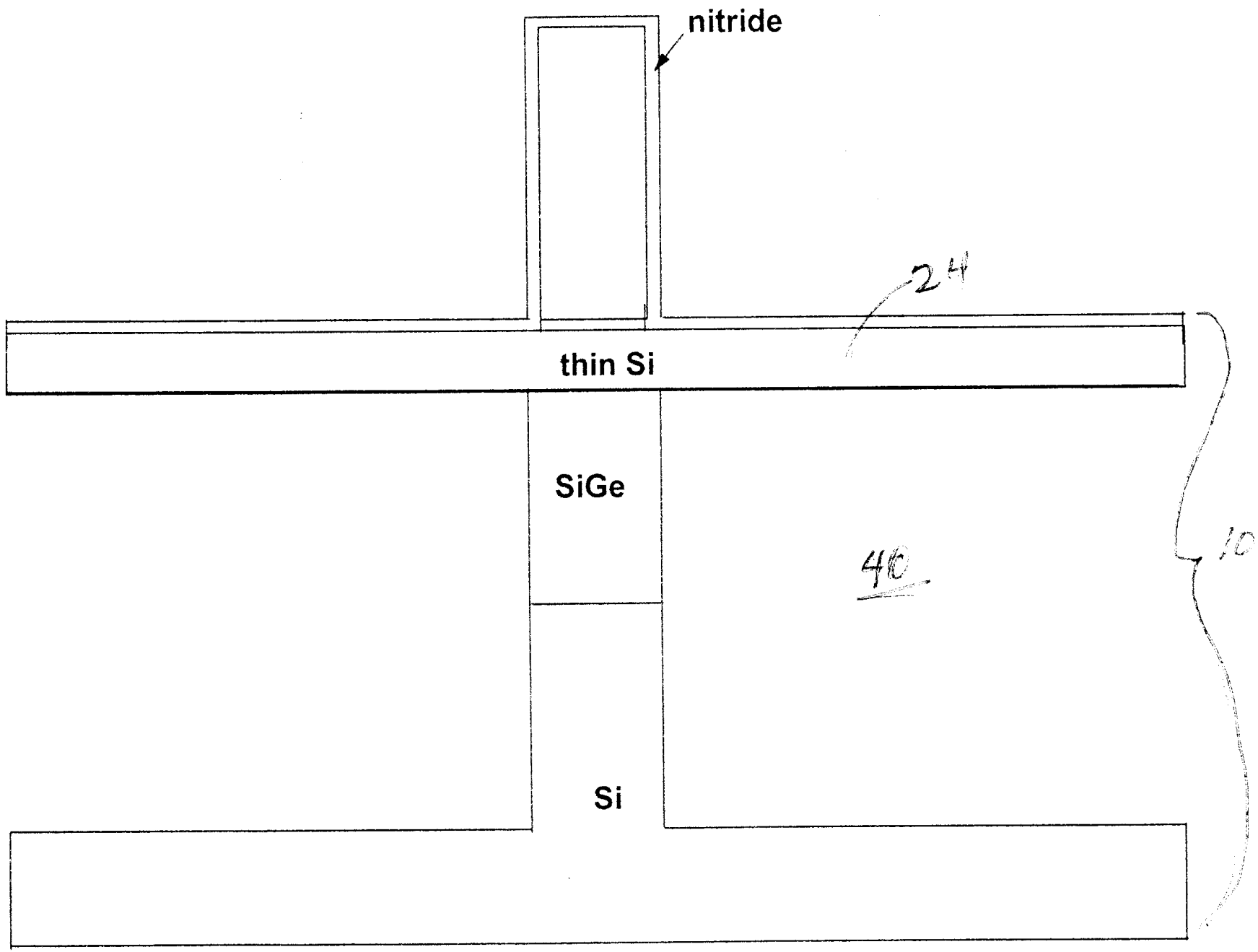


FIGURE 4

Step 4 Oxidation and etch thin oxide. Since oxidation rate in SiGe is about 3.5 times faster than Si, the thickness of oxide on the SiGe sidewall is thicker than that on pure Si. After the etch there is oxide layer left over on the SiGe sidewall

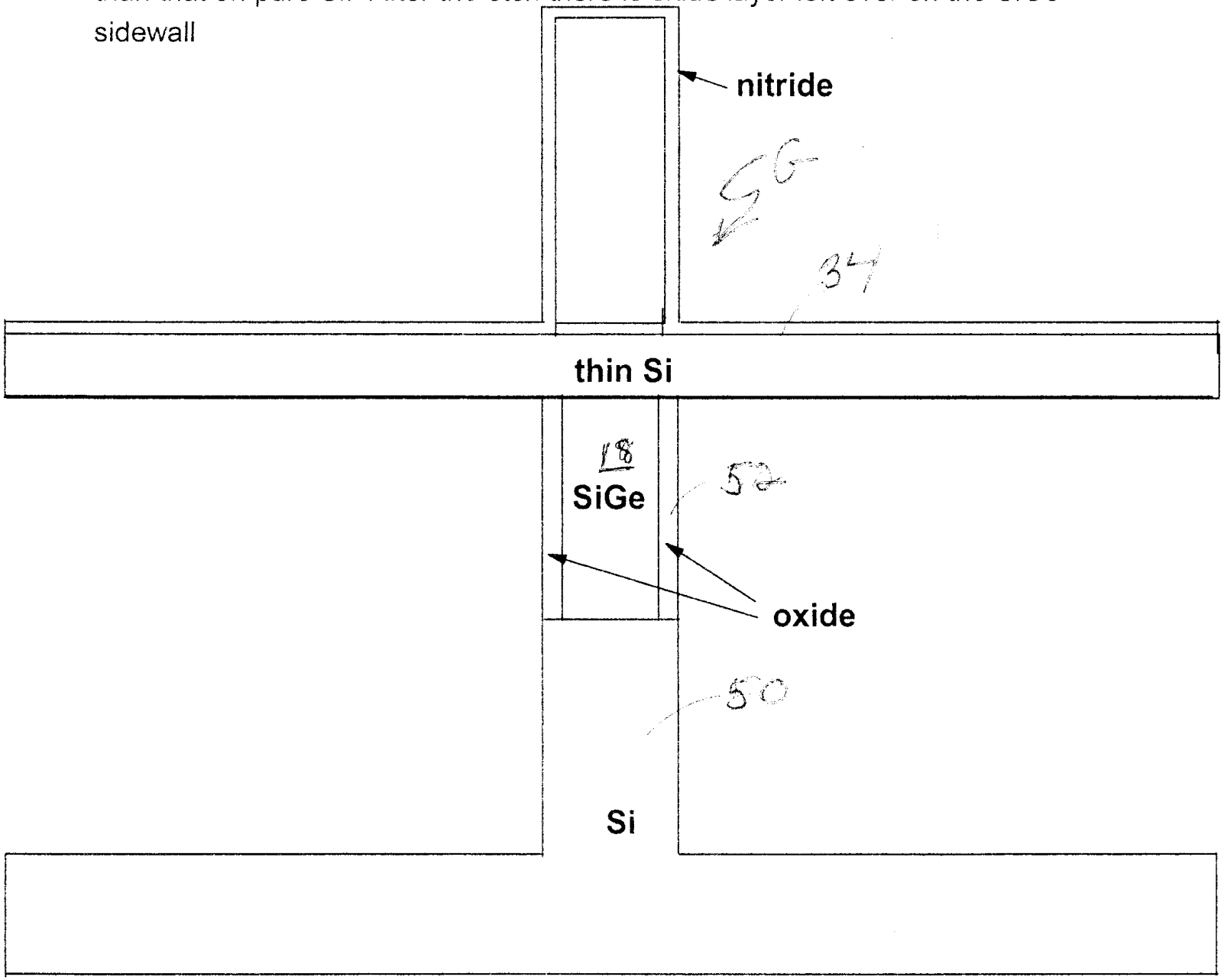
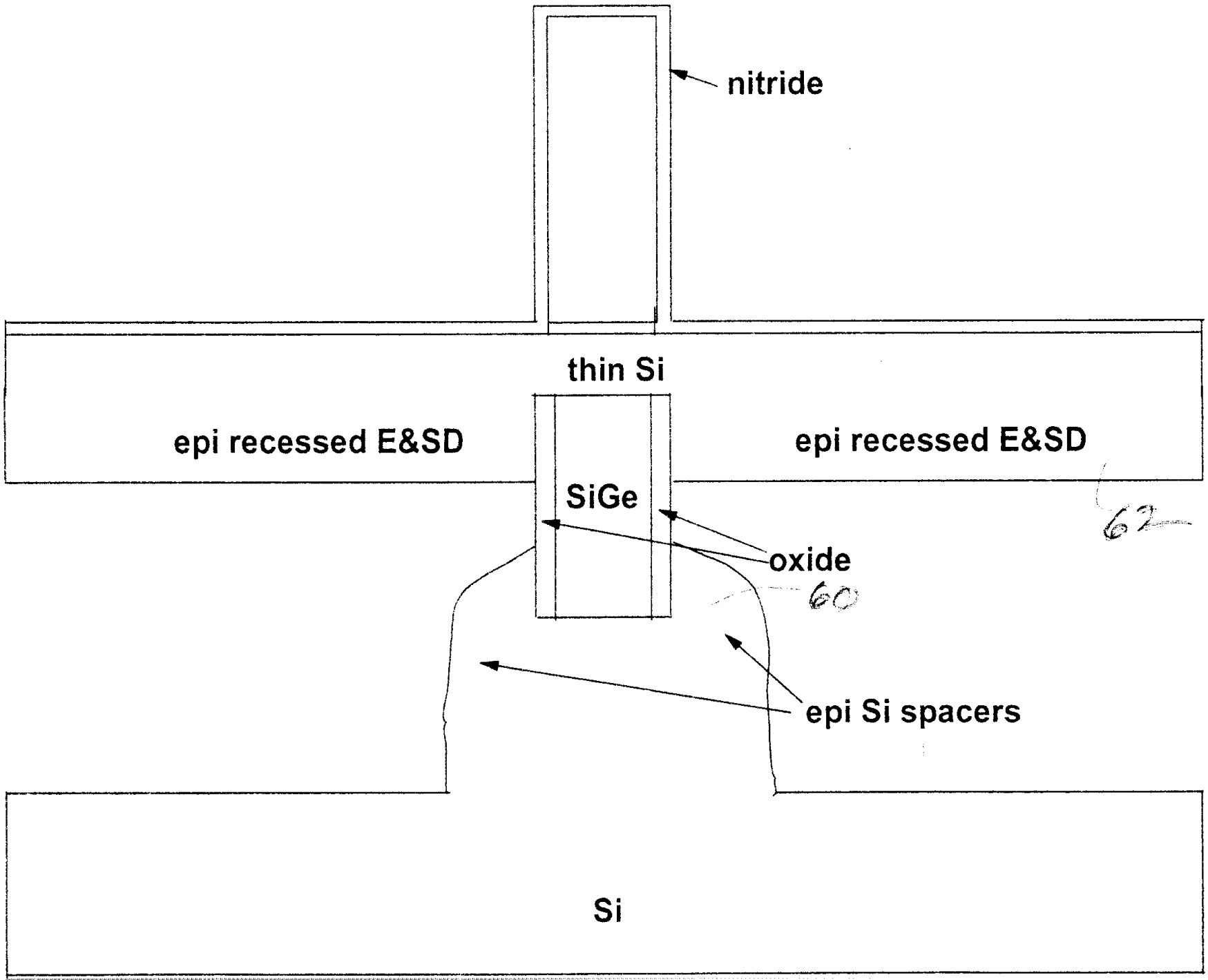


FIGURE 5

Step 5 Selective epi Si



Step 6 To make sure the epi Si spacer not shorting with the epi recessed E&SD, we do As ion-implantation one more time

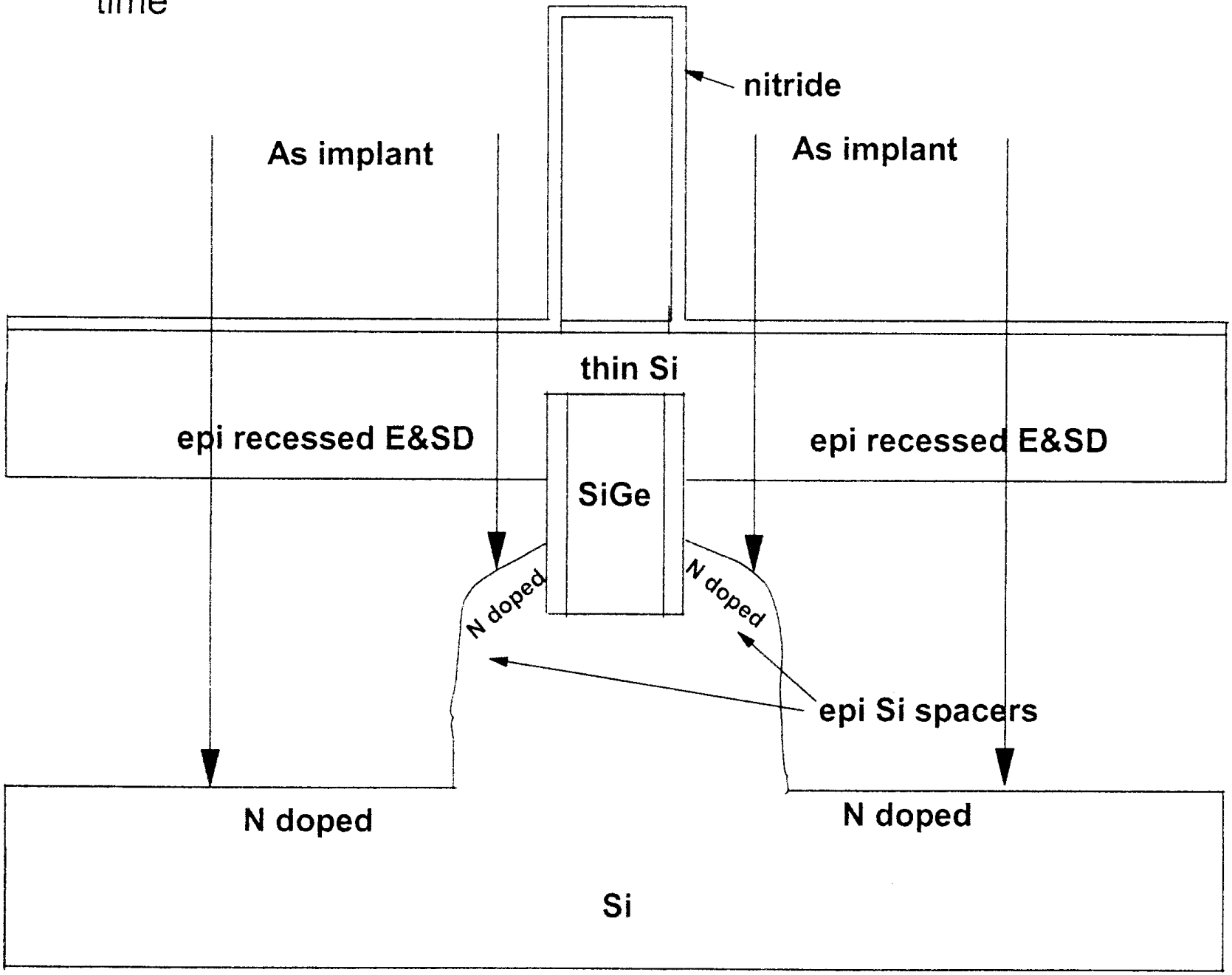


FIGURE 7

Step 7 Etch the N doped area and refill the void by insulator (say oxide). (We also can etch the oxide on the SiGe sidewall and depsoit low-k material or even leave them opened to improve short channel effect)

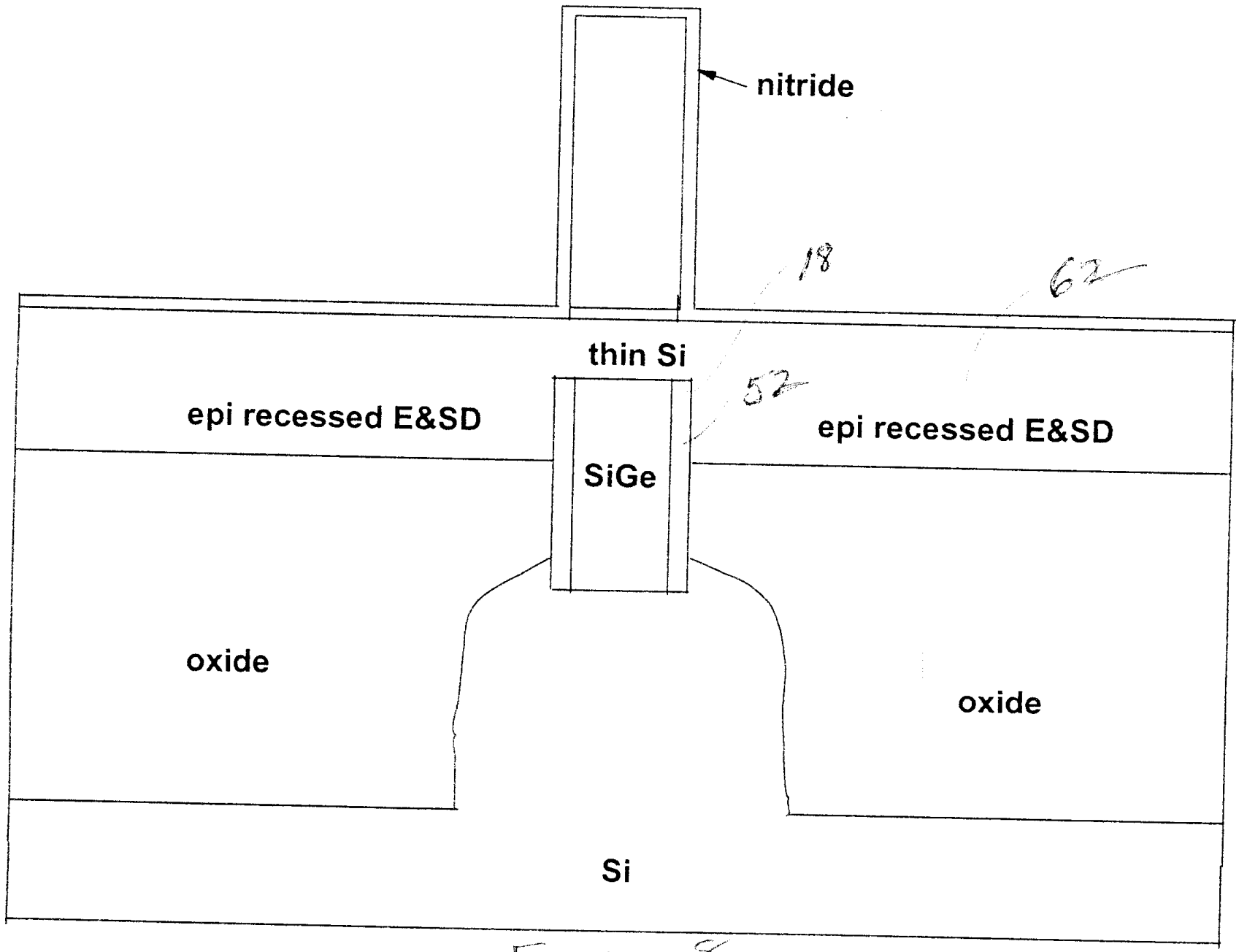


FIGURE 8

Structure Claimed

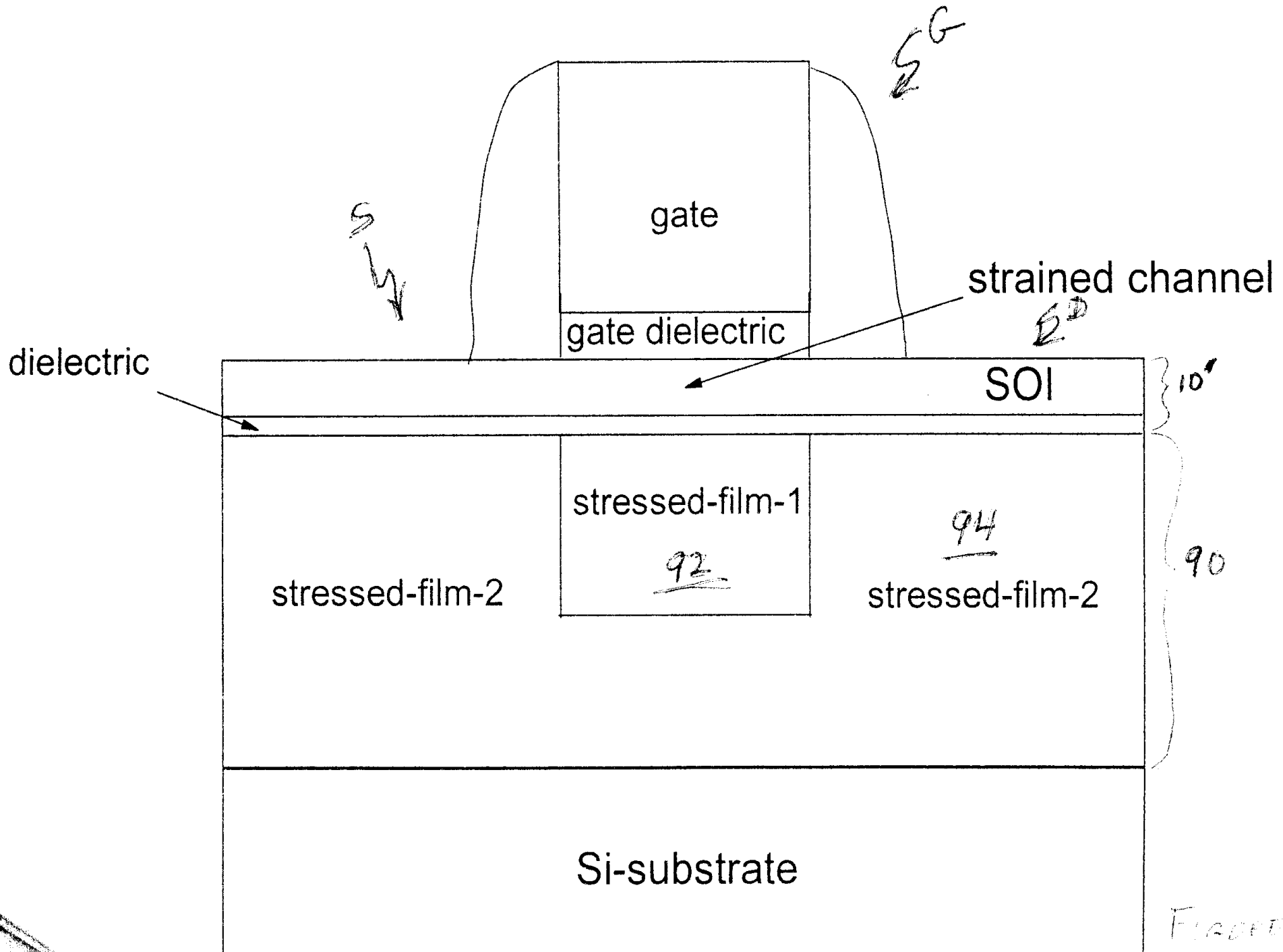


FIGURE 9

Step 1 Start with a bonded wafer with SOI/oxide/large-grain-p-Si/SiGe/Si-substrate

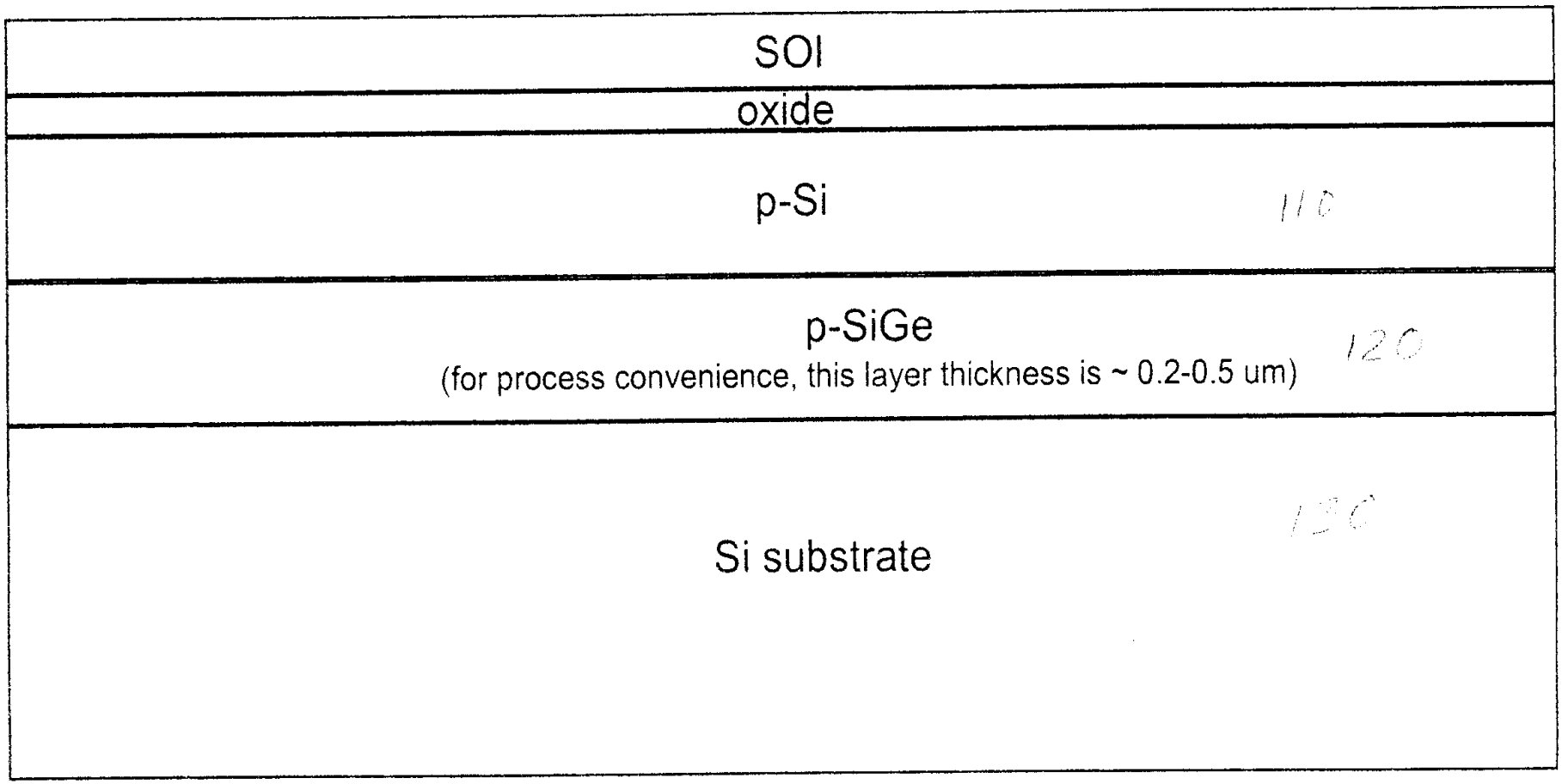


Figure 10

Step 2 Form trench and thin nitride spacer to protect gate oxide. Pattern gate with a thick oxide cap to prevent ion-implantation used for etch to go into the gate. Boron implantation into the large-grain-p-Si layer only.

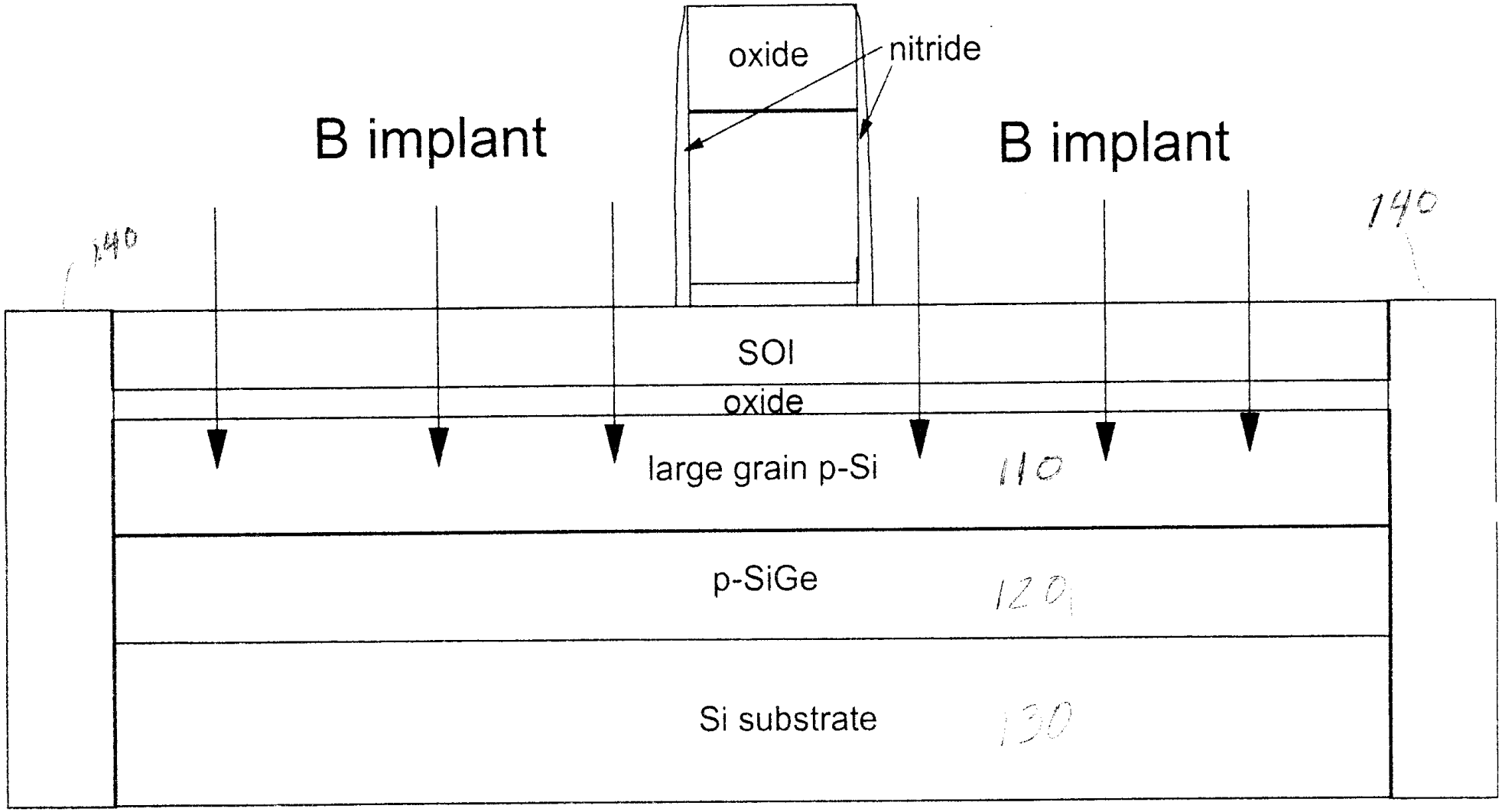


FIGURE 11

Step 3 Pattern photoresist and etch down one trench (say left trench) to the level below the Si-substrate surface

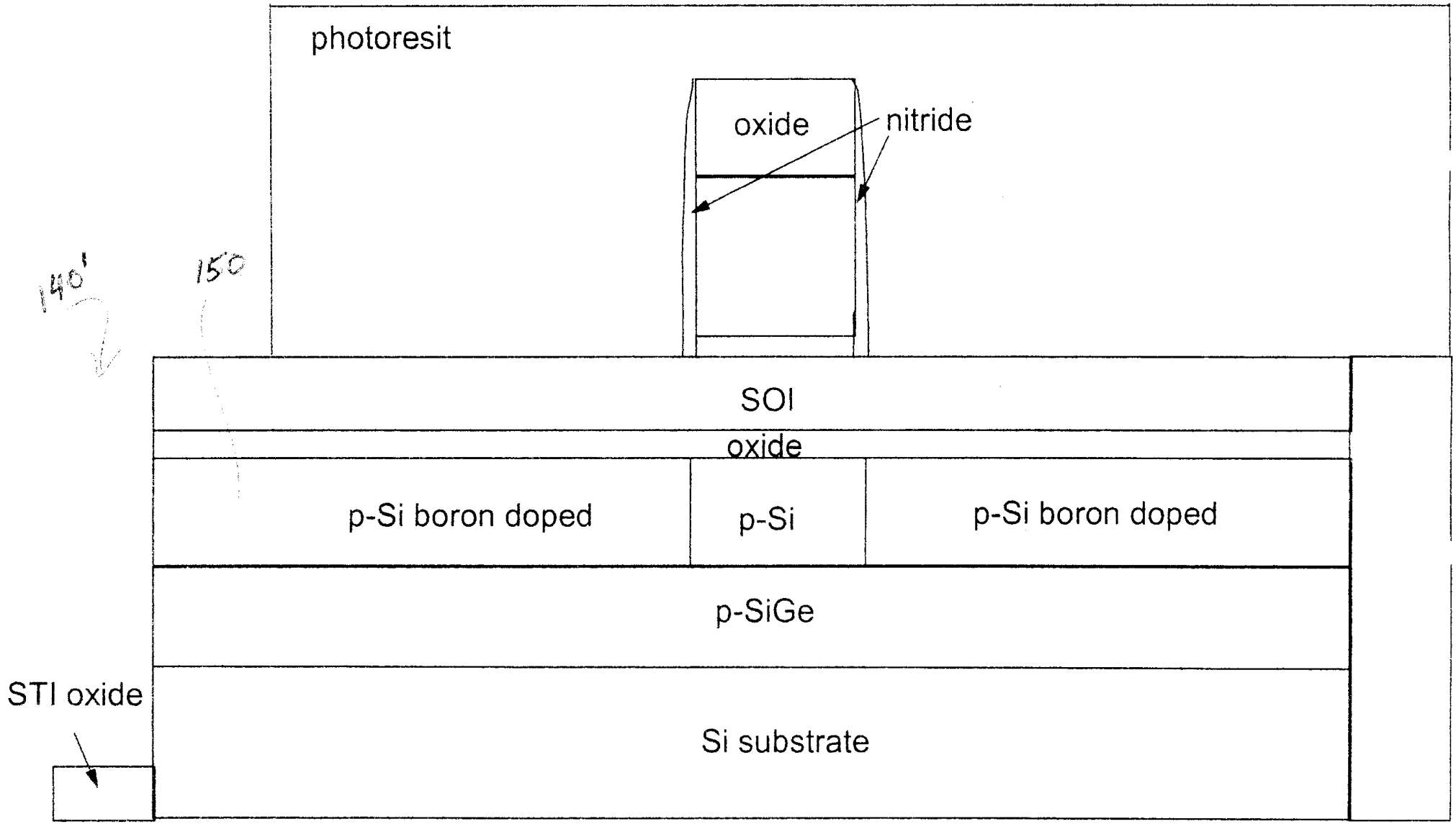


FIGURE 12

Step 4 Selective etch the p-SiGe under the p-Si and remove the photoresist

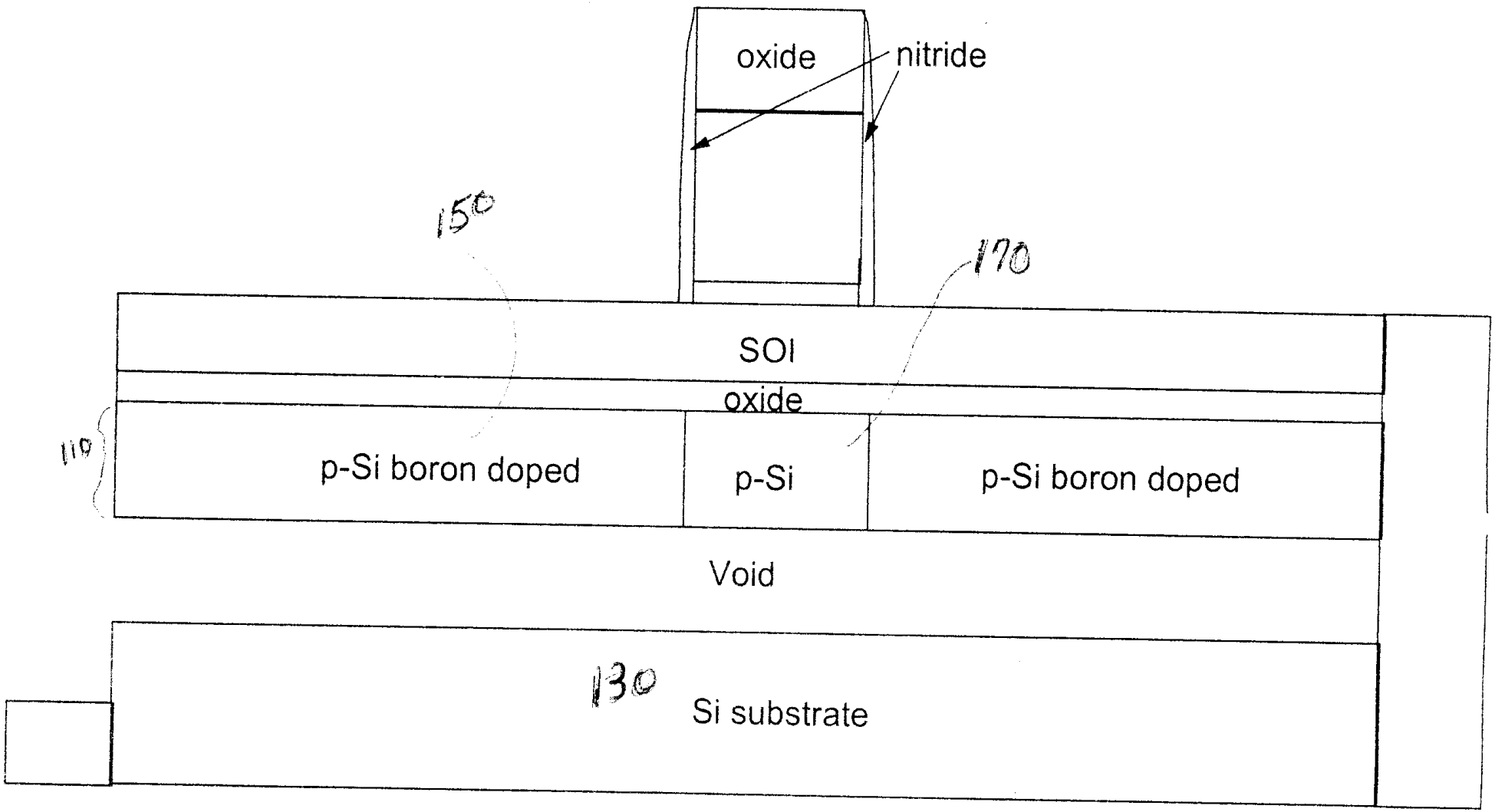


FIGURE 1C

Step 5 Directive deposit oxide to protect SOI from being etched and selective etch the undoped p-Si under the gate. Deposit stressed film

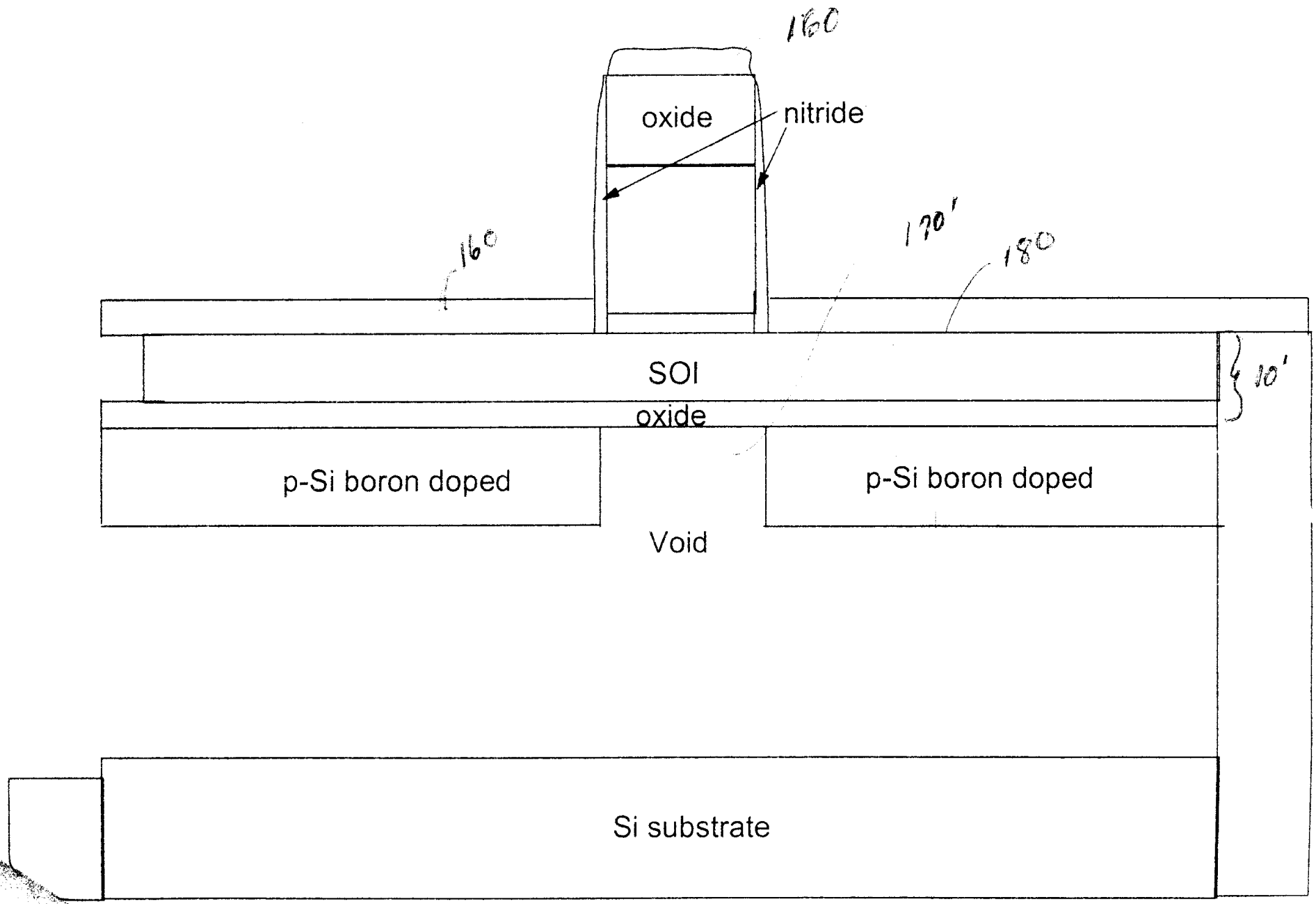


FIGURE 14

Step 6 Deposit stressed-film-1. Regarding the stress in the film, for nfet prefer compressive and pfet tensile.

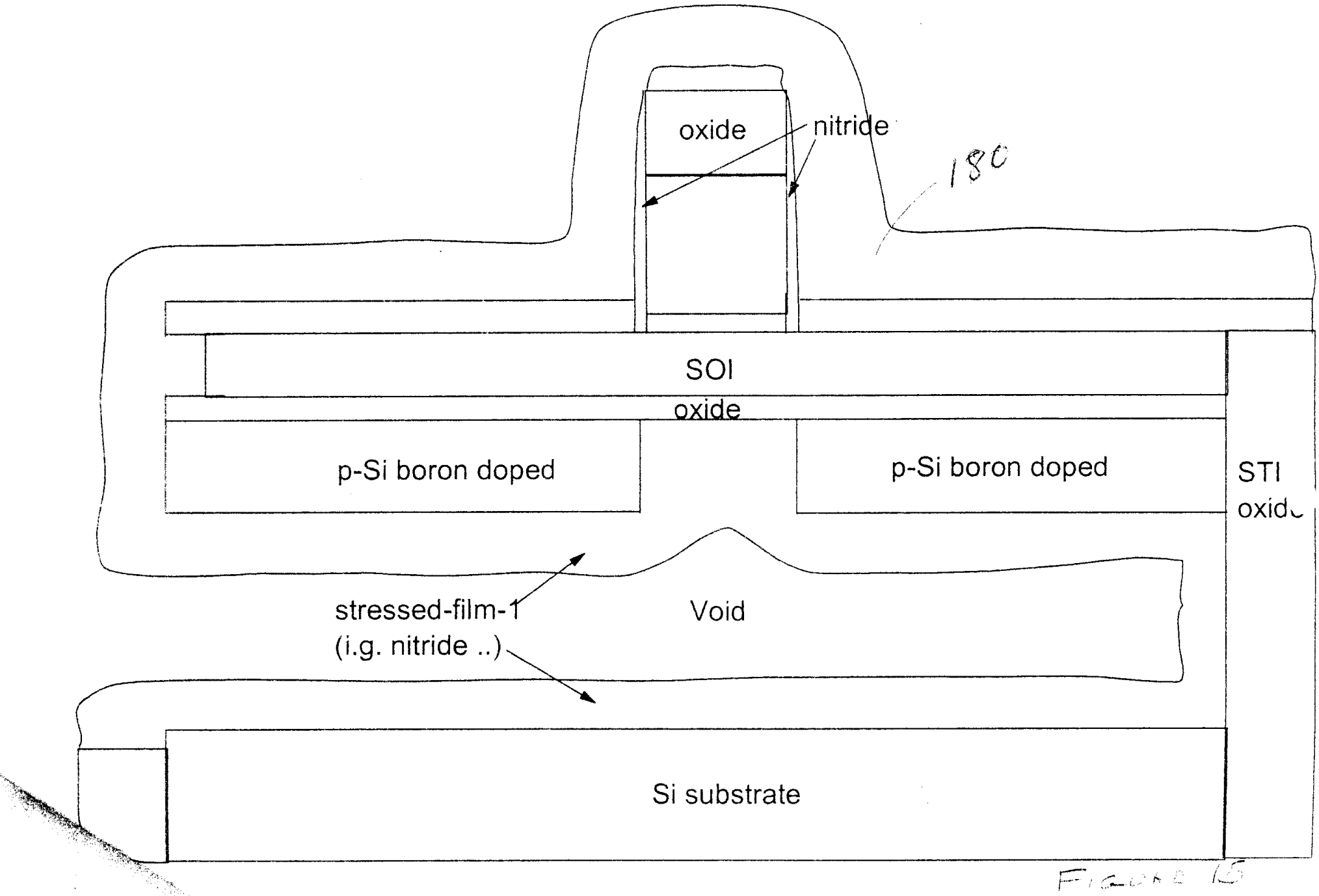


FIGURE 15

Step 7 Wet etch the stressed-film-1.

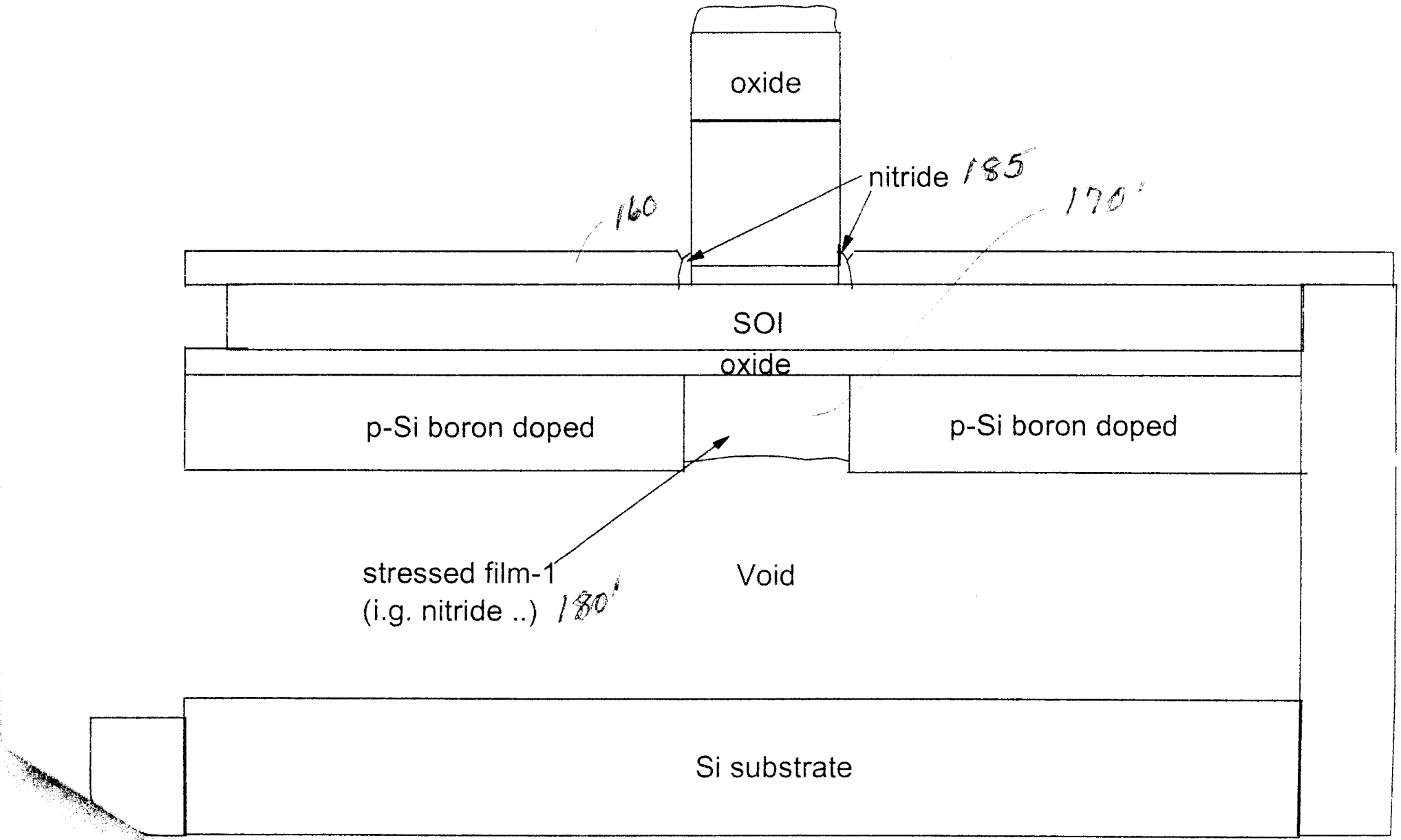


FIGURE 16

Step 8 Arsenic implantation to turn the boron doped p-Si into n-type p-Si and anneal in order to etch the p-Si away.

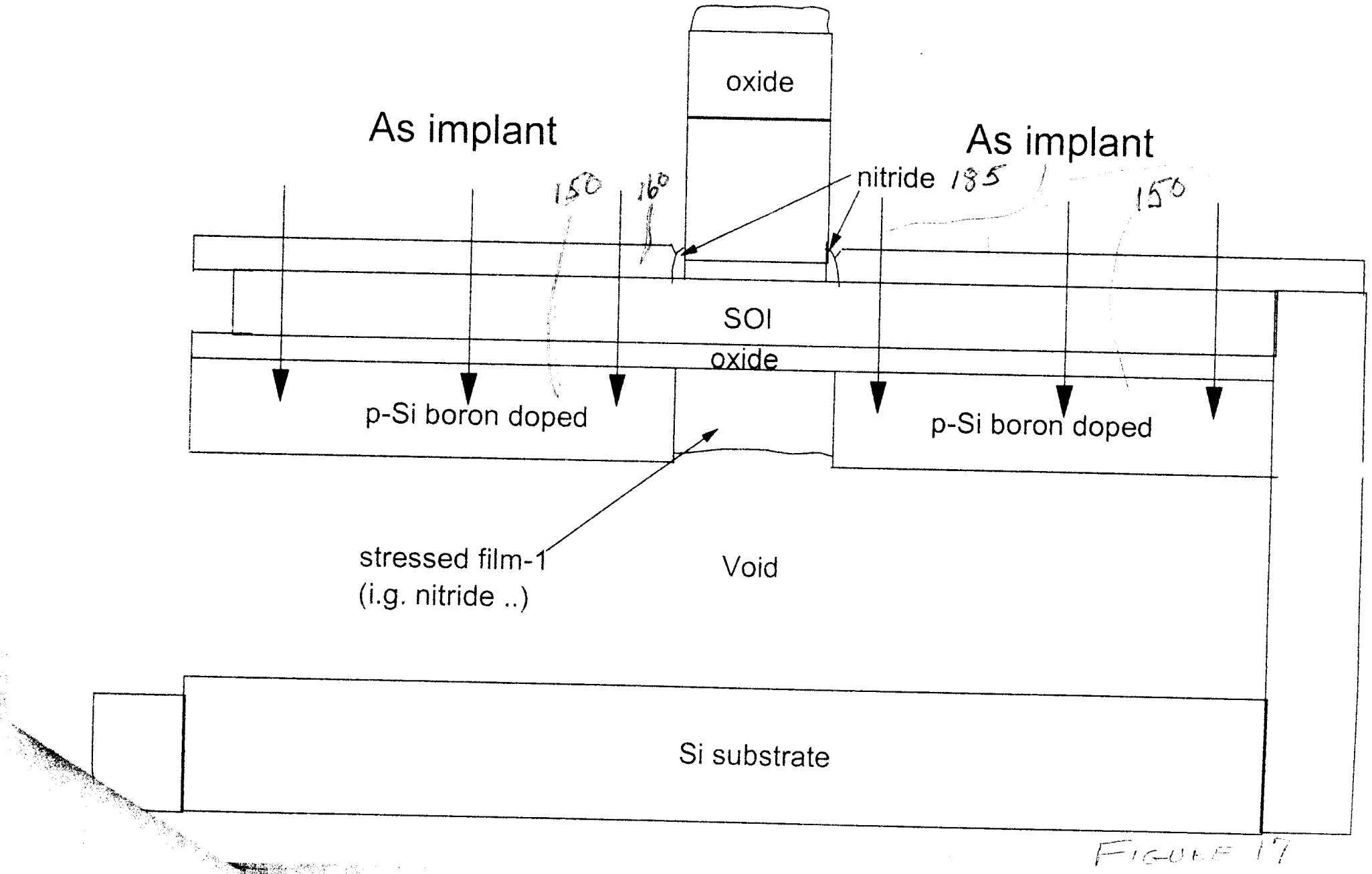


FIGURE 17

Step 9 Etch the n-type p-Si, deposit stressed-film-2 to fill the void and wet etch stressed-film-2. This time the stress in stressed-film-2, for nfet prefer tensile and for pfet compressive.

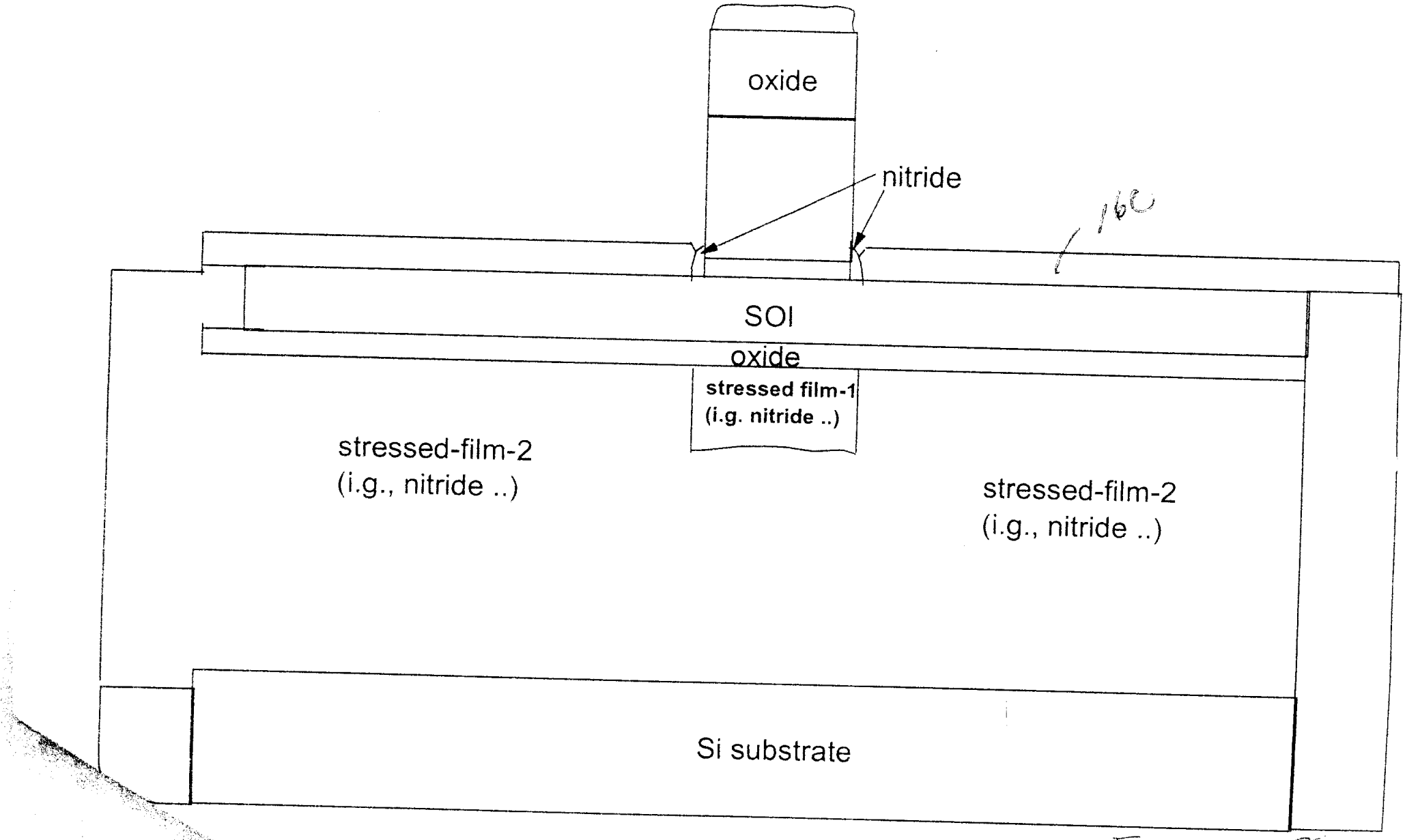


FIGURE 18

Step 10 After direct etch the oxide, one can follow conventional process to make nfet and pfet.

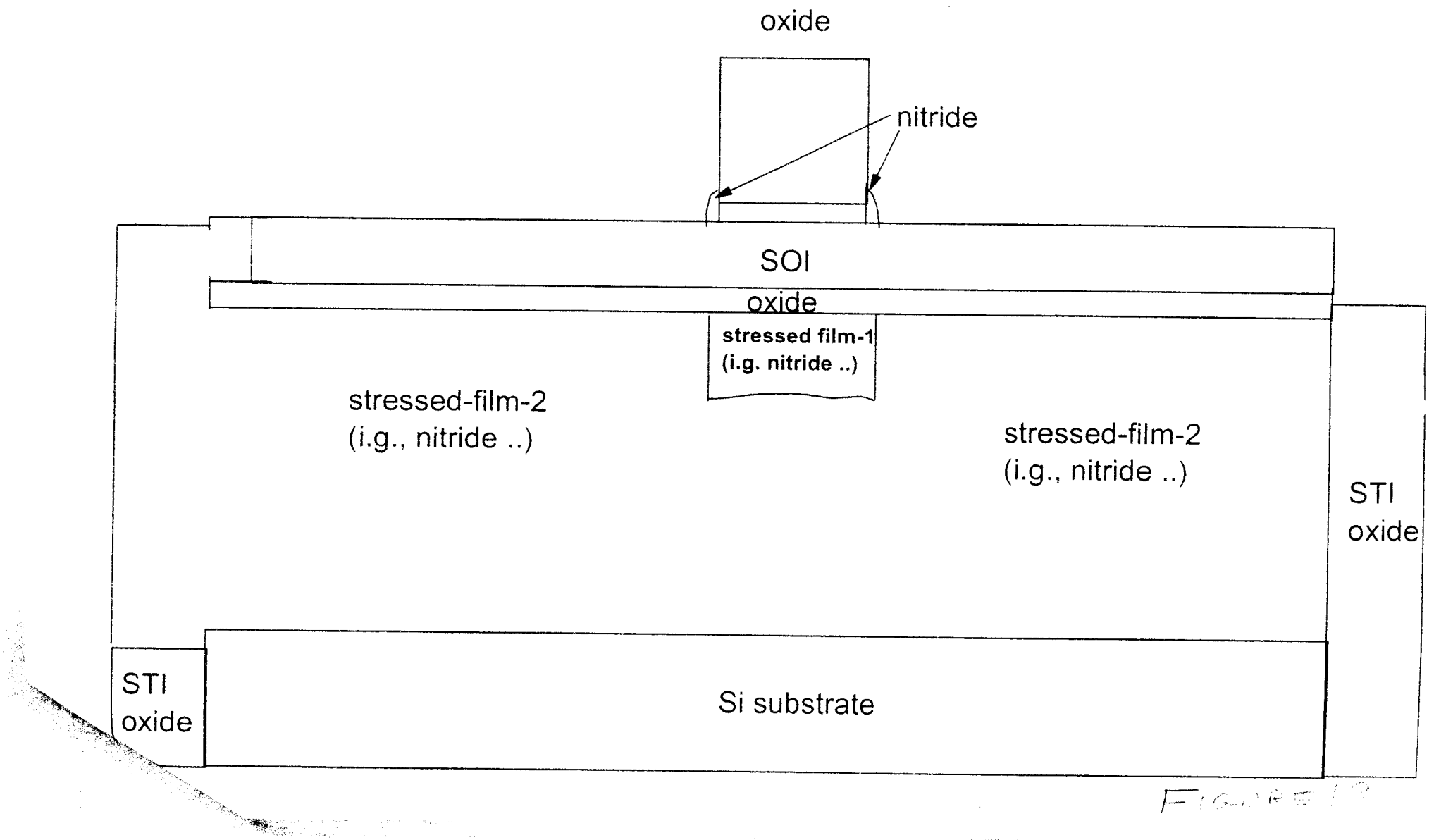


FIGURE 10

Step 1 Start with a conventional wafer, epi thin SiGe layer and then epi relaxed Si layer

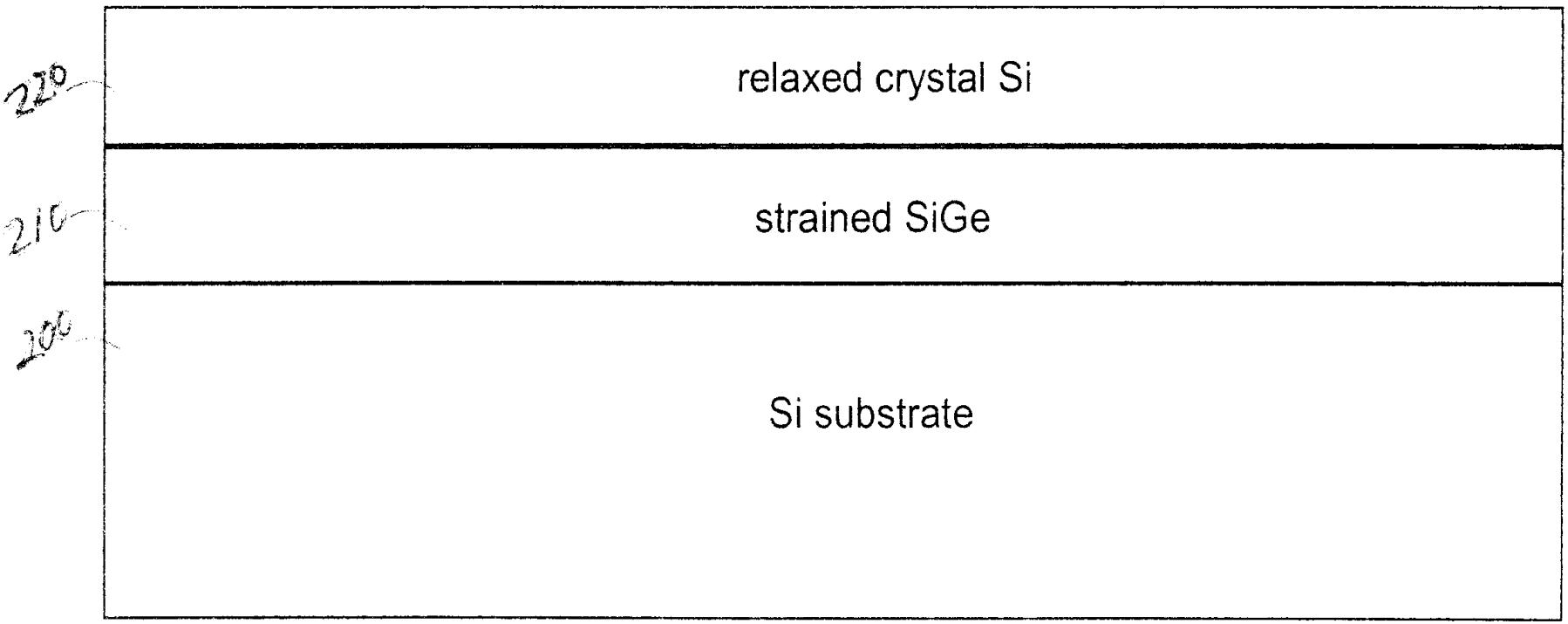


FIG. 2C

Step 2 Form trench and build a pMOSFET with all dopants are in place. Start with a conventional wafer, epi thin SiGe layer and then epi relaxed Si layer

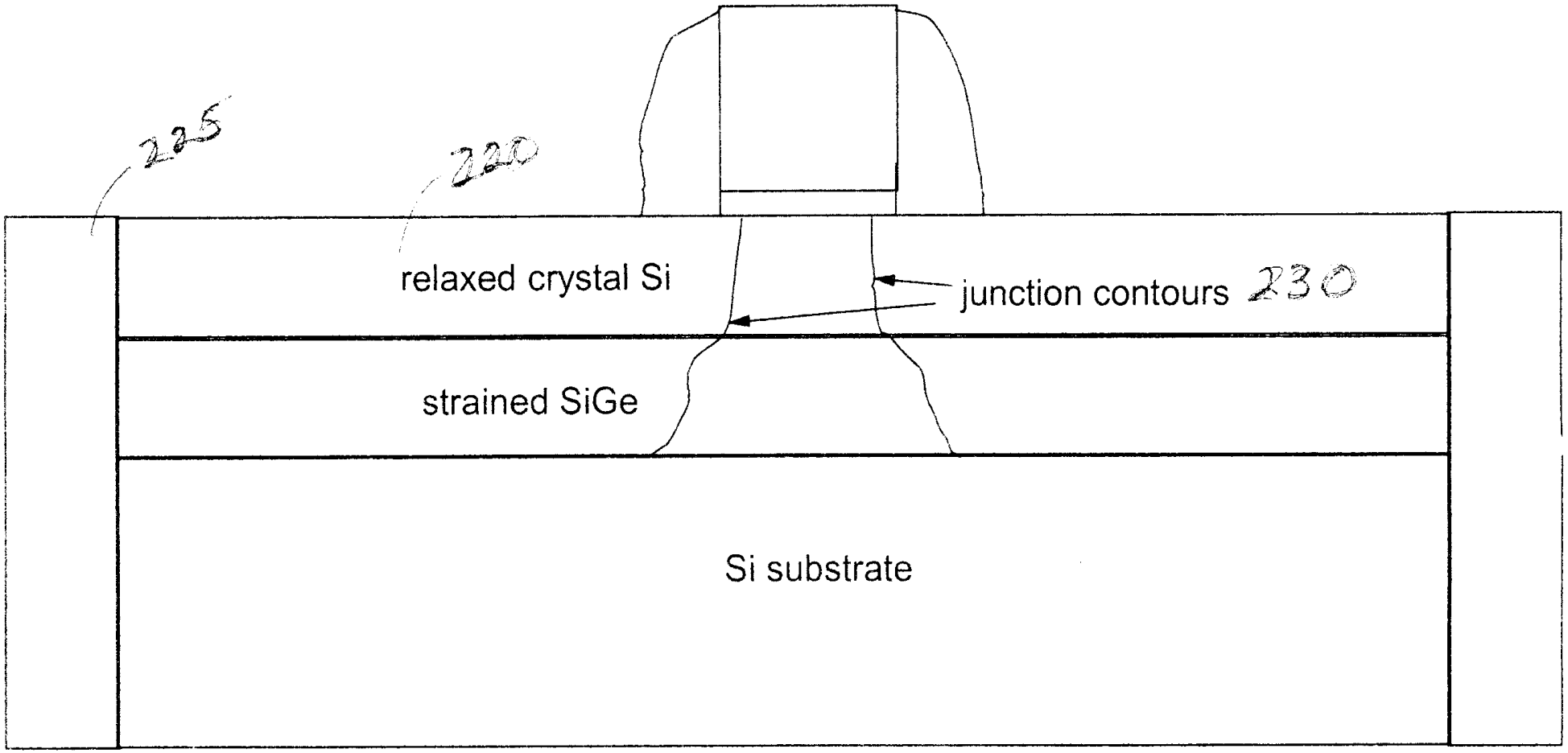


FIGURE 21

Step 4 Deposit CA liner, cover one trench and etch down another open one (say left trench) stopping on Si substrate. Form a nitride spacer on the sidewall of the relaxed Si and strained SiGe.

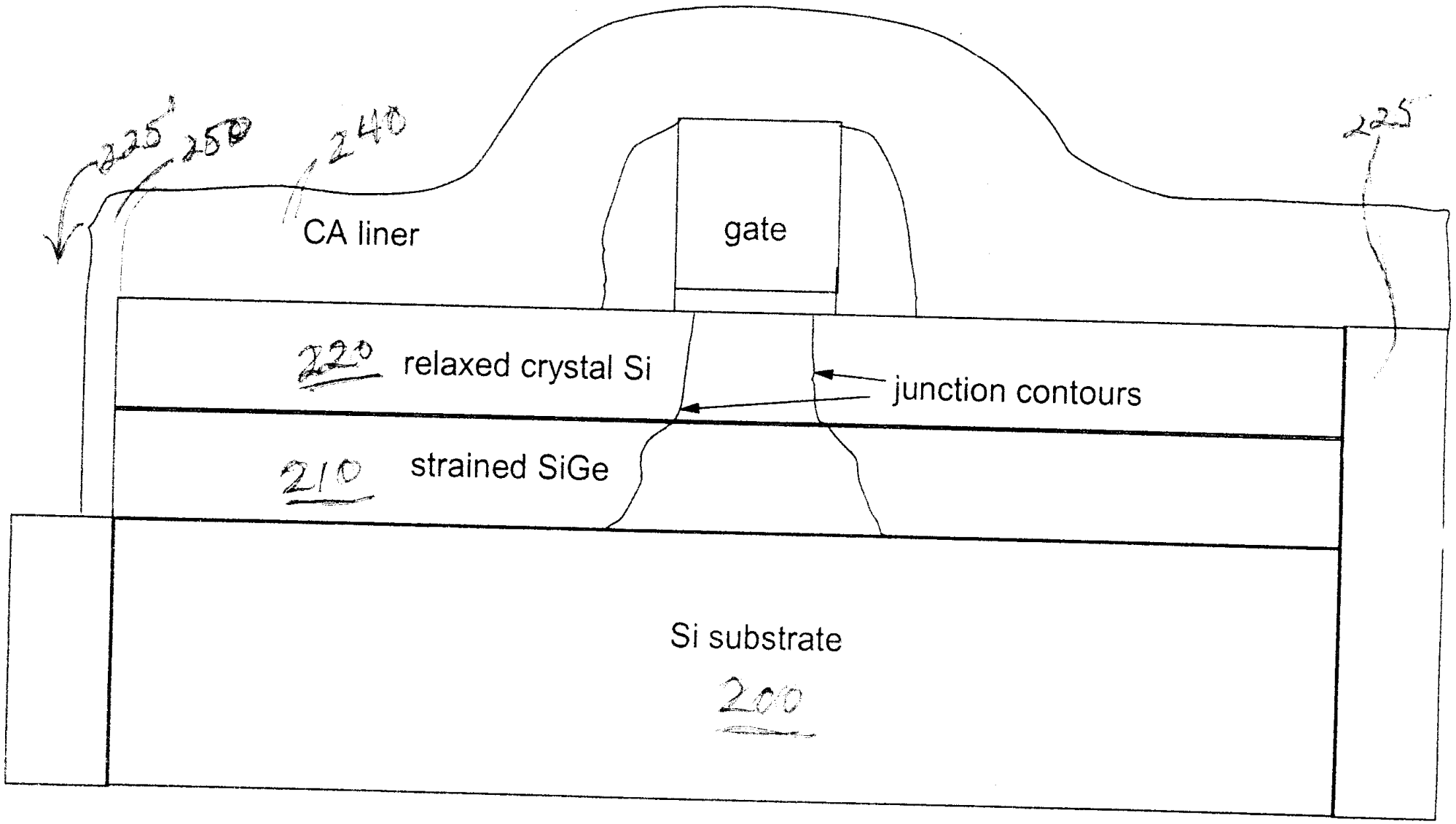


FIGURE 22

Step 4 Continue etch the STI oxide of the left trench, selective etch Si under the strained SiGe layer.

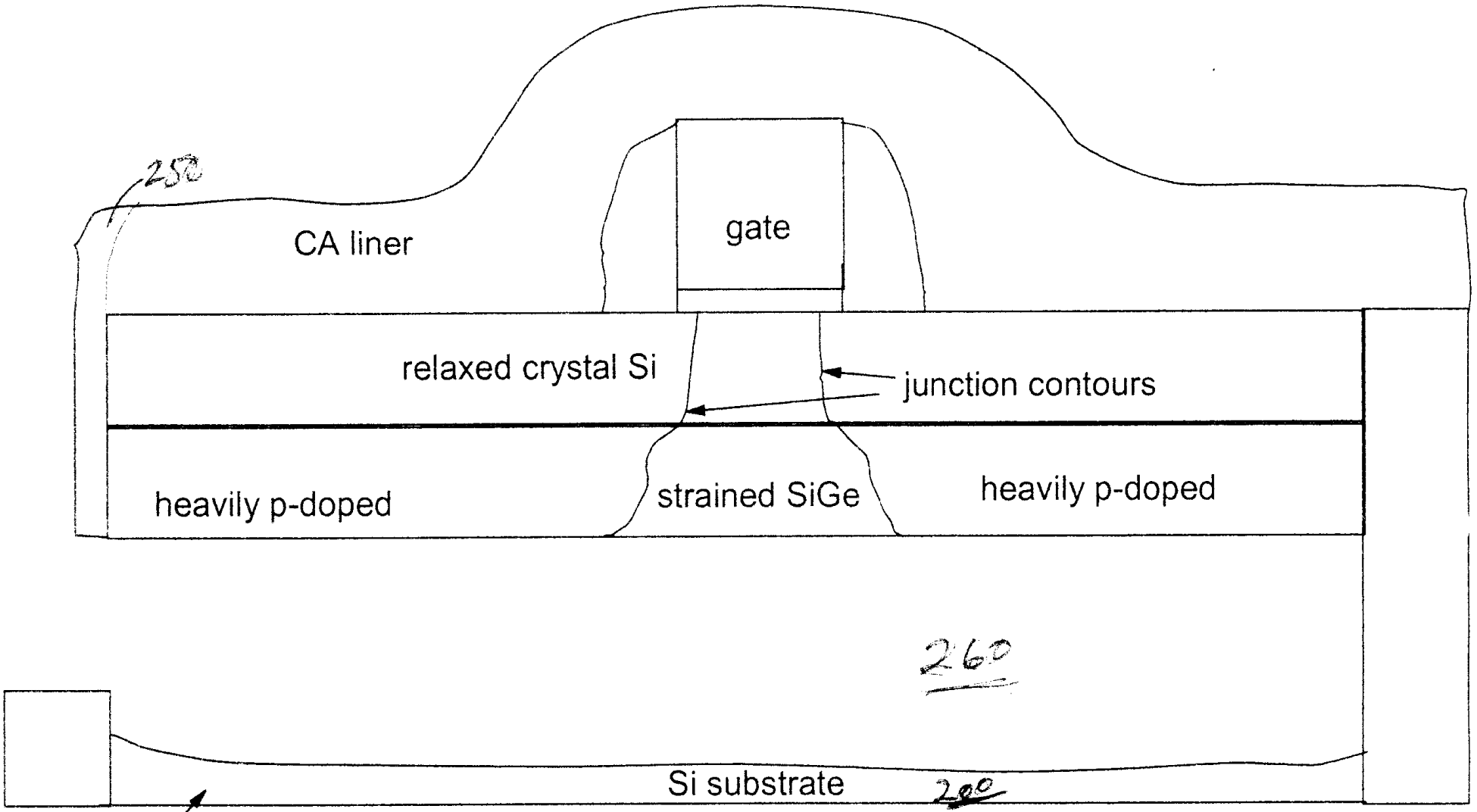
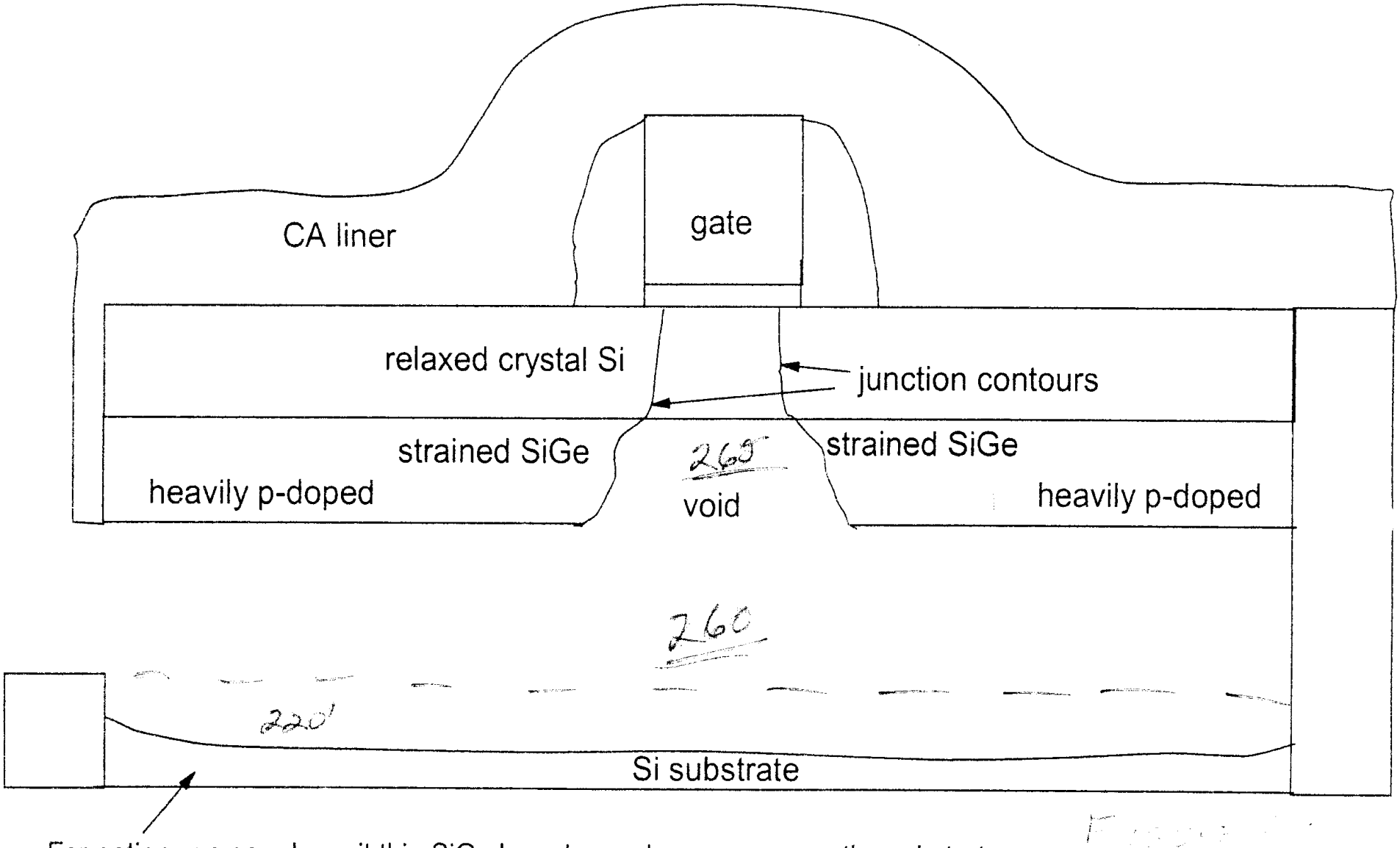


Figure 3

For option, we can deposit thin SiGe layer here when we prepare the substrate.
In this case, we can get flat plane after wet etch Si between the two SiGe layer

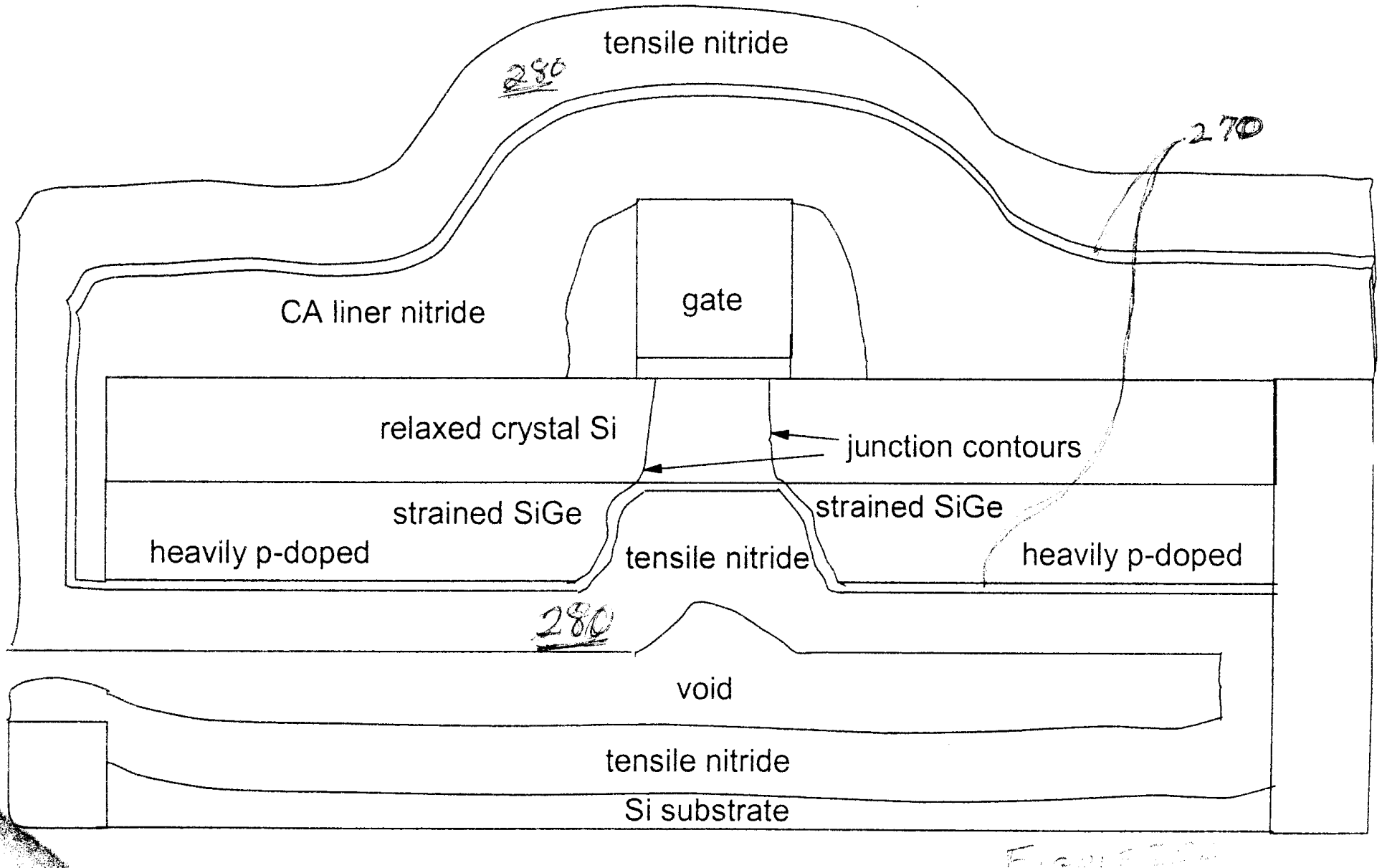
Step 5 Selective etch the n-type strained SiGe under the gate. In this case, the strained SiGe film in the extension and SD area can apply stress to the channel.



For option, we can deposit thin SiGe layer here when we prepare the substrate.
In this case, we can get flat plane after wet etch Si between the two SiGe layer

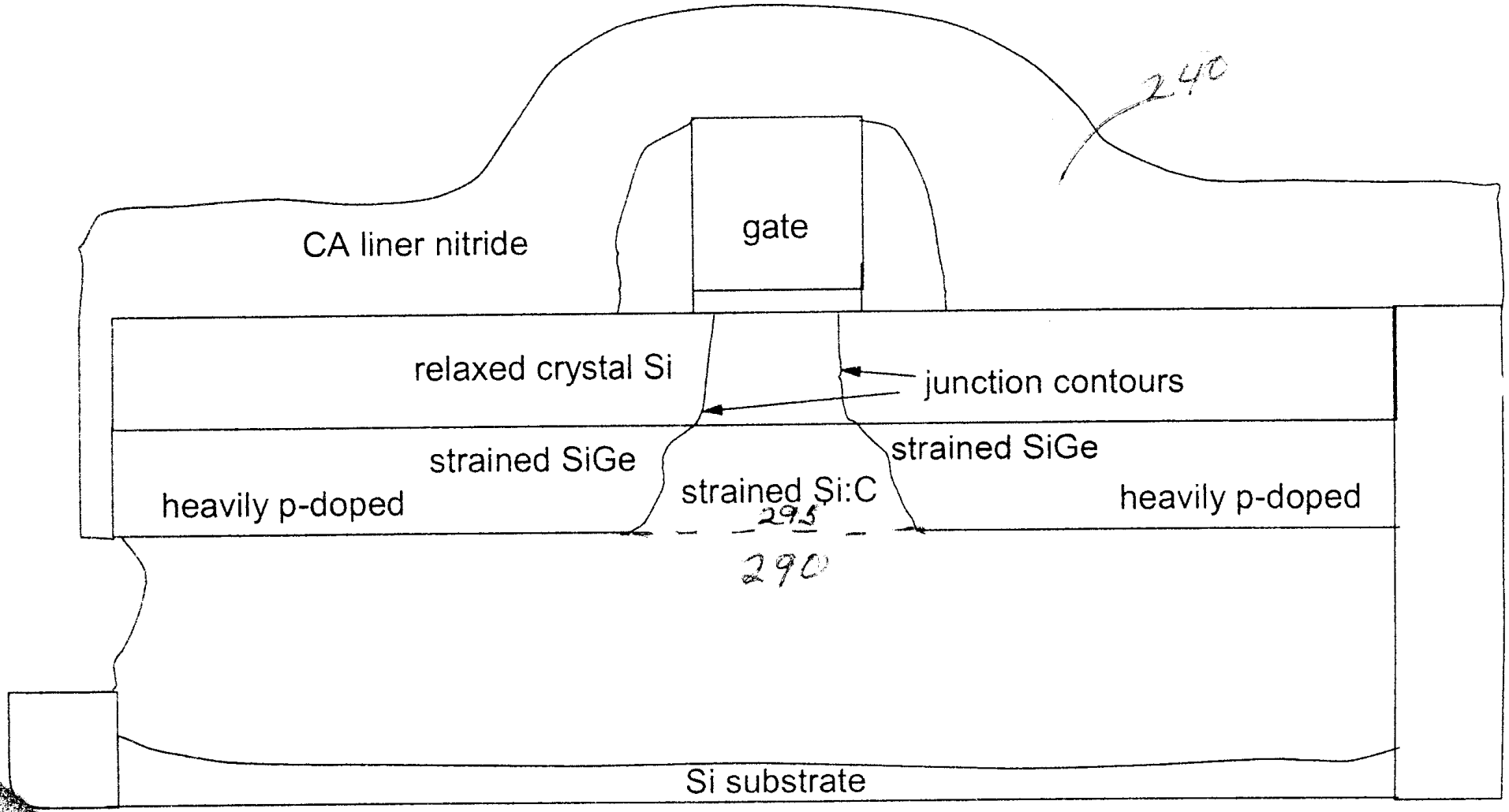
Step 6 For SOI and SON device:

Deposit thin oxide in order to protect the surface under the channel and then deposit tensile nitride film to add additional compressive stress to the channel. If no nitride is deposited, one get silicon-on-nothing (SON) device.



Step 6 For bulk device:

Epi Si:C to add additional compressive stress to the channel. Direct etch the Si:C on the top of CA liner. In this case, the Si:C is not subject to high temperature process and the stress in the Si:C is maintained. This has advantage over methods using Si:C as substrate before SD RTA. (Another option for preventing the Si:C growing from the strained SiGe, one can do oxidation first. In this case, the oxide on the SiGe is much thicker (due to oxidation on SiGe much faster) than that at the bottom of Si channel. One can wet etch the oxide at the channel bottom, but remain some oxide on the strained SiGe. after this the Si:C film is growed.)



Simulations of stresses in a Pfet channel (Lpoly = 60 nm):

Compressive stress along the channel (Tsi = 10 nm) cut at 5nm belowe the gate oxide after etch the strained $Si_{0.75}Ge_{0.25}$ (~2GPa stress) under the gate and then deposit compressive 40 nm nitrdie film (film stress ~1.5GPa).